Stacked Nb-$MoSi_2$-Nb Josephson Junctions for AC Voltage Standards

Paul D. Dresselhaus, Yonuk Chong, and Samuel P. Benz

***Abstract*—Superconductor-normal metal-superconductor (SNS) Josephson junctions have proven to be a critical technology for voltage standards. NIST has used SNS junctions for both dc and ac programmable voltage standards. Previous devices have used primarily PdAu as a normal-metal barrier material. In this paper we present measurements of circuits having $MoSi_2$ barriers. Stacking enables the junctions to be packed more densely, thus increasing design flexibility and margins for the microwave circuits. In this work, measurements are presented from two- and three-junction stacks for application to ac Josephson voltage standards, which show output voltage and distortion near our best previously published results.**

***Index Terms*—Digital-analog conversion, Josephson arrays, superconducting devices, superconducting films, thin film devices.**

I. Introduction

STACKED arrays of superconductor-normal metal-superconductor (SNS) Josephson junctions have become the primary technology for applications of ac quantum voltage standards at NIST. Non-stacked SNS junctions have been widely used in both dc and ac voltage standard applications because of their stability and noise immunity (providing large operating margins) [1]. Stacked junctions, because of their inherent high linear density, have already generated higher voltage for our programmable dc voltage standard [2]. In this work, we introduce the use of $MoSi_2$-barrier stacked junctions for applications in ac voltage standards.

SNS junctions have previously proven to be critical to ac Josephson systems [3]. The large critical current, high uniformity, and characteristic frequency of several gigahertz combine to yield large operating current margins in ac voltage standard circuits. The main limitation of these circuits has been the limited output voltage (usually less than 0.25 V) while retaining the operating margins. The use of stacked junction arrays has been suggested as a straightforward way to increase this voltage. Stacked junction materials for voltage standard applications have been previously studied [4].

Stacked SNS arrays have also been fabricated using NbN-TiN_x-NbN junctions for voltage standard applications because they operate at temperatures up to 10 K [5]. While these circuits show promise for dc operation, the Nb-$MoSi_2$-Nb material system seems to show the most promise for tall stacks (more than two junctions/stack) because it has the potential to provide lumped element arrays at microwave frequencies [6]. The work in this paper focuses on $MoSi_2$ barrier devices.

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II. Devices

Double- and triple-stacked junction arrays were fabricated on oxidized Si substrates 76 mm in diameter. Details of the fabrication process for the double- and triple-stacked programmable circuits are reported elsewhere in these proceedings [2]. The stacked junctions were assembled into arrays of 1052 (short) or 2104 (long) stacks that were embedded in a coplanar transmission line with 16 μm wide inner conductor, 7 μm spacing, and 100 μm wide outer conductor. The short arrays had a single 180° bend in the transmission line, while the long arrays had three bends. All transmission lines are terminated with a 50 Ω on-chip resistor. Each array has two taps at both the top and bottom of the junction array such that a four-point measurement can be made and the common-mode signal from the termination resistor is not measured. Two identical arrays are coupled with the bottom taps, and complementary microwave signals are applied to each array in order to double the output signal [7]. Further increases in voltage output using this method are limited only by the number of microwave lines into the cryostat as well as the equipment needed to produce the signals.

Current-voltage characteristics for each array were measured as shown in Fig. 1 for a short triple-junction stacked array. These data were fit to the RSJ model to derive the normal-state resistance, $R_n = 4.5$ mΩ, and thus the characteristic voltage, $I_cR_n = 37.5$ μV. The sharpness of the onset into the voltage state is a measure of the uniformity of critical current in the array. Non-uniform junction properties typically manifest themselves as a rounding of the voltage state transition, or a hump in the current-voltage characteristics, which indicates that one junction in each stack has a different critical current. The array in Fig. 1 shows such a hump, indicating that devices on this wafer have two distinct critical currents that differ by $\sim$10%. Because this has not been observed for other stacked junction wafers, it is due most likely to some anomaly in the growth of these multilayers.

A continuous microwave signal was then applied to count the number of junctions in the array by verifying that the first Shapiro step voltage is $nNfh/(2e)$, where N is the number of junctions, n is the step number, $h/(2e) = 2.07$ mV/GHz is the flux quantum value, and f is the frequency of the applied microwave. Our standard criterion used to determine flatness is a voltage difference of less than 1 μV across the step. The first-step ($n = 1$) voltage and the zero-step ($n = 0$) voltage were then measured to determine thermal voltages and microwave-induced voltage shifts. Thermal voltages may be subtracted or

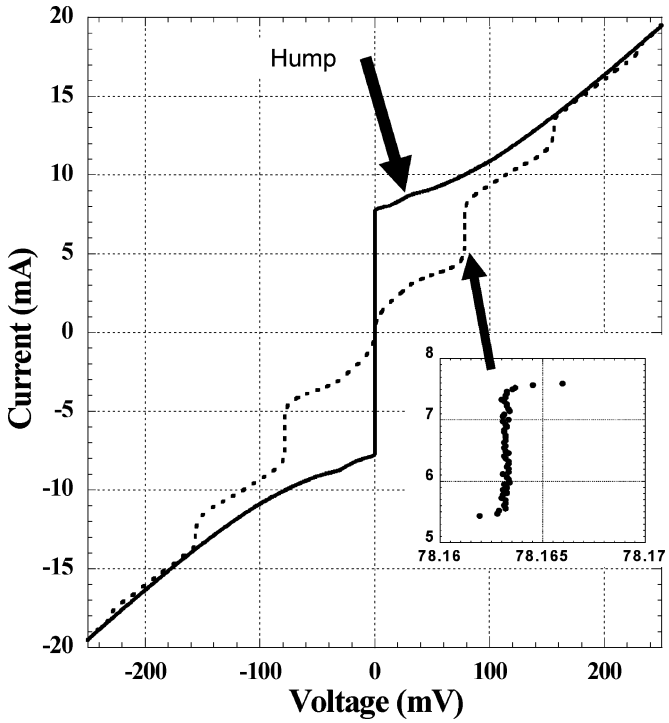

Fig. 1. Current-voltage characteristics of a three-junction stack array with 3150 junctions. The solid trace shows the dc characteristics, while the dashed line is taken with 12 dBm of 12 GHz microwave radiation. The inset shows an expanded view of the $n = 1$ Shapiro step, which is flat to within 1 μV over a range of more than 1 mA. The upper arrow points to a hump indicating that the devices on this wafer have two distinct critical currents.

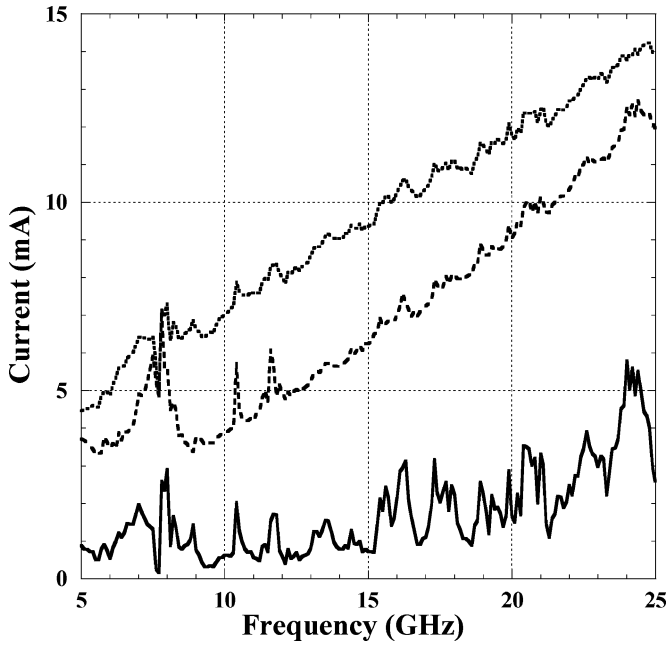

Fig. 2. Frequency dependence of the $n = 0$ and $n = 1$ Shapiro steps for a two-junction stack array with a total of 4208 junctions. The solid trace below shows the zero step, while the upper two traces denote the upper and lower limits of the $n = 1$ step. The power was linearly ramped with frequency so as to compensate for the junction dynamical properties.

ignored for ac work, but the microwave-induced voltage shifts indicate fabrication errors and the circuit must be discarded.

In order to test the on-chip microwave filters, the Shapiro steps were measured over a broad frequency range. As the microwave source was stepped in frequency, the limits of the first and second Shapiro steps were measured and plotted as in Fig. 2 for a two-junction stacked array. The figure shows a broad operating range from 9 GHz to 25 GHz over which the first step range is at least 1 mA. Such a broad operation band is desirable for ac Josephson voltage standards, because these arrays are driven over a broad range of frequencies.

Fig. 2 also shows no step range near 8 GHz. This indicates that there is some deviation from the designed microwave distribution in this narrow band. Because the zero step also increases, much lower microwave power is reaching the array, and the radiation that does reach the array has a poor distribution across the array, leading to a smaller first step current range. There are also similar smaller features in the data, but these depend on the circuit and fabrication, while the 8 GHz feature is common to many designs. We believe that this common feature may be caused by off-chip microwave launches.

III. Measurements and Discussion

The ac Josephson voltage standard, also called the Josephson Arbitrary Waveform Synthesizer (JAWS) system, uses a digital-to-analog synthesis technique in which fast electrical pulses drive a single flux quantum through each junction in an array [8]. Complex waveforms may be realized using a simple algorithm to generate a digital code that is loaded into the circulating memory of a microwave digital code generator. A microwave sine wave is added to the digital code to make bipolar signals and to increase the output voltage [9]. Microwave digital pulses are combined with a microwave sine drive and subsequently dc blocked. The microwave signals are applied to the Josephson circuit through a transmission line from room temperature to liquid helium. A low-frequency tone is directly added to the circuit bias leads to compensate for the dc blocks on the microwave lines. The JAWS system is more completely described in [10].

Once a circuit has been verified for dc and microwave operation with all junctions operating properly over a broad frequency range, the circuit is tested with the JAWS system. It is of particular interest to determine how the stacked-junction arrays perform in comparison to the previously used PdAu-junction arrays. Note that the frequency range shown in Fig. 2 is not the entire extent of the frequency response of the Josephson circuit. In order to show large operating margins, the circuit must respond to the entire spectrum of the applied delta-sigma code, which generally spans from dc to 20 GHz. Thus, even at frequencies at which the microwaves will not produce a Shapiro step, the circuit must uniformly deliver this broadband signal to the entire array. Some circuits with excellent Shapiro steps failed to yield large JAWS operating margins because they proved to be highly reflective at a narrow frequency band near 500 MHz.

The canonical test of a JAWS circuit is the application of a digital code of 3 000 064 bits representing a single cycle of a sine wave (e.g., a 10 GHz code rate implies $f_{sine} = 15$ GHz, and a 3333.262224 Hz sine waveform). The peak output voltage is then determined by the modulator algorithm, the microwave sine frequency, and the number of junctions. For the standard

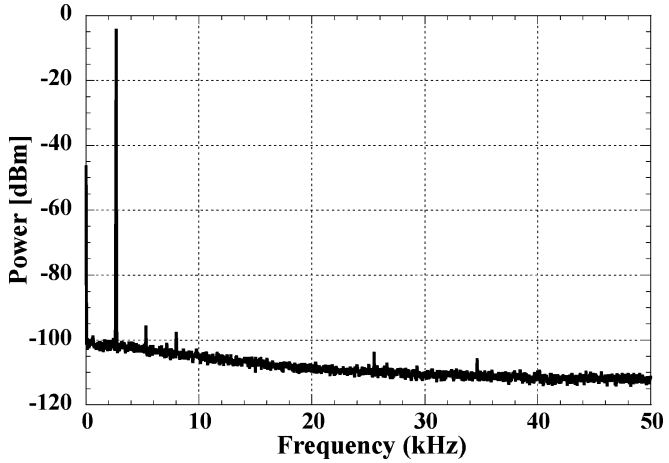

Fig. 3. Spectrum of a 200 mV peak 2.6 kHz sine wave produced from two coupled 4208 junction double-stacked arrays (for a total of 8416 junctions). The distortion harmonics are -92 dBc, indicating that the circuit still has a small operating margin.

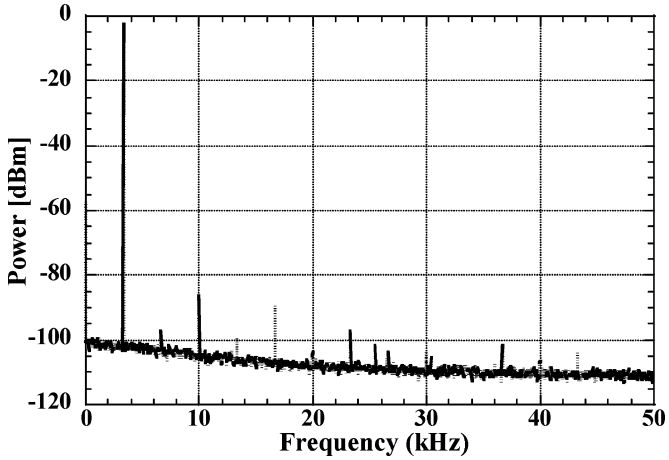

Fig. 4. Spectrum of a 248 mV peak 3.3 kHz sine wave produced from two coupled 4208 junction double-stacked arrays. The maximum distortion harmonic is -86 dBc, indicating that the circuit has no operating margin.

algorithm, we have a peak voltage $V_{peak} = 0.95 * f_{sine} * N_{JJ}/K_{J-90}$, where f_{sine} is the frequency of the microwave sine drive, N_{JJ} is the number of junctions in the array, and $K_{J-90} = 483.5979$ GHz/μV is the Josephson constant. The value of 0.95 is the maximum possible to keep the modulator algorithm stable. By fixing the value of f_{sine}, the output frequency and the peak voltage amplitude are also fixed.

Fig. 3 shows the power spectrum of the output from a JAWS circuit driven with a code rate of 8 GHz, a microwave drive of 12 GHz, and a 2.6 kHz sine-wave output. The peak output voltage from the 8416 double-stacked junctions arranged in two series-connected arrays is 200 mV. The distortion is -92 dBc (dB below the fundamental tone peak voltage). This is close to our record output voltage of 242 mV with -93 dBc distortion using PdAu barrier junctions [11], [12]. However, if the frequencies driving this device are all increased by 25%, so that the code generator is clocked at 10 GHz, then the voltage increases to 248 mV (Fig. 4). Although the peak output voltage is significantly increased, the distortion has increased to -86 dBc, well above the noise floor of the spectrum analyzer. This indicates that the circuit no longer has operating margins at this drive frequency, Another measurement of the long double-stacked array at $f_{sine} = 14.25$ GHz gives an output voltage is 235 mV with a distortion of -91 dBc. This is just below the best output of our PdAu barrier device [12].

Another measure of the operating margin is the so-called "flat spot" measurement, in which the output is measured with μV/V precision while varying all the relevant inputs [12]. While the best output voltage for a PdAu barrier circuit is 242 mV, the highest voltage that had a flat operating spot at μV/V precision was 200 mV. Flat-spot measurements have yet to be performed on $MoSi_2$ barrier devices.

A summary of the maximum harmonic distortion is plotted in Fig. 5 for all the correctly operating two- and three-junction stack circuits. The figure shows a loss of operating margin at near the 0.25 V peak level. Note that the arrays in Fig. 5 have different total junction numbers. In general, short arrays with fewer junctions tend to have larger operating margins, while the long

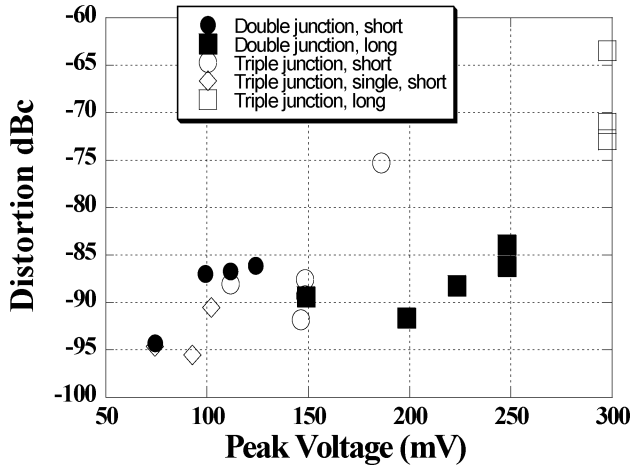

Fig. 5. Distortion summary of two- and three-junction stacked array circuits. The open and filled circles represent data from two coupled "short" arrays, the squares indicate "long" arrays, and the diamonds indicate a single "short" array. Double-junction stacks are indicated with filled shapes, while the open shapes represent triple-junction stacks. Both wafers had characteristic voltage ~ 37.5 μV.

arrays have small or no margins. The longest arrays in terms of junction count have too many junctions attenuating the pulse amplitude, such that the last junctions in the array are not driven with a pulse large enough to drive a single flux quantum through each junction.

Achieving higher output voltage simply by increasing the junction number seems to be possible until the total number of junctions in a single array exceeds about 5000 junctions. At this point the operating margins shrink rapidly to zero. Microwave attenuation in the array is the most likely cause; a 5000-junction array has a normal resistance of over 20 Ω, which is comparable to the 50 Ω transmission-line impedance. Further increasing the junction count in a single array is not likely to work unless R_n is also decreased.

Another method of increasing the output voltage is by using a higher drive frequency to the array, but this is limited by several factors. The on-chip microwave structures have more nodes at higher frequencies, degrading the microwave

power uniformity in the array. The open circles in Fig. 5 represent this effect: even though there are only 3156 junctions in each triple-junction stacked array, the distortion rises if $f_{sine} > 15$ GHz (V > 186 mV). Also, the devices should have a larger characteristic voltage I_cR_n for higher-frequency operation; if I_c is fixed, this leads to smaller junctions, which suffer more from nonuniformity in the etch process. The double-stacked junctions of Fig. 5 show better distortion than the triple-stacked junctions. The short double stacked arrays work well up to $f_{sine} = 15$ GHz, while the long double-stacked arrays work only to $f_{sine} = 12$ GHz. Junction nonuniformity and nodes in the longer microwave structures are probably culprits in this increased distortion. For triple-stacked arrays, only the short (1052 stacks) arrays had operating margins, even at the lowest speeds. This was expected, because the long triple-stacked arrays had over 6000 junctions, which cause too much microwave loss in the signal reaching the last junctions in the array.

One factor that could help increase operating margins is further improving the uniformity of junctions. Other work [6] has shown that up to 15 junction stacks may be etched with good uniformity. The bimodal distribution of critical currents on this wafer, visible as a hump in the $I-V$ curve of Fig. 1, shows that junction uniformity in these devices could be improved. Also, using a better junction-etch recipe will provide a more uniform stack and thus higher margins. Nonetheless, the performance of these arrays for ac voltage standards is at near-record levels, and the stacked-array technology is promising for ac voltage standards.

IV. Conclusion

Double- and triple-stacked junction arrays have been fabricated and measured for ac voltage standard applications. The circuits have shown good margins and near-record output voltages. Voltages up to 200 mV have been produced with distortion of -93 dBc with long double-stacked arrays. The $MoSi_2$ barrier SNS junction technology shows the potential to surpass our traditional PdAu barrier for Josephson voltage standards.

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